ABSTRACT OF THE DISCLOSURE

The data processor has a set-associative cache memory capable of performing associative operation using tag information for an indexed cache line. The cache memory includes way prediction part for performing a selection of a way based on the prediction in parallel with the associative operation, generation part for generating way selection determining information based on the associative operation using the subsequent access address during a penalty cycle caused by a prediction miss of the way prediction part, and control part for making a way selected for the subsequent access address after the penalty cycle on the basis of the way selection determining information. Since a way to be hit at the subsequent cache access can be predetermined during the preceding penalty cycle, the cumulative number of penalty cycles can be reduced.